11. (Amended) A fabrication method of a semiconductor device comprising:

a first step of forming a first insulating film on a substrate, said substrate having a semiconductor region;

a second step of forming a second insulating film on the substrate, said second insulating film being of a different material than the first insulating film and serving as a polishing stopper;

a third step of forming by an etching process an opening in the second insulating film, wherein a part of the second insulating film remains within said opening;

a fourth step of forming a metal film on the second insulating film and the opening, wherein the metal film has a polishing rate greater than that of the second insulating film;

a fifth step of polishing the metal film to expose a surface of the second insulating film etched in the third step and to form a flat plane comprising the exposed surface of the second insulating film and a polished surface of the metal film; and

a sixth step of washing the polished surface of the metal film by (i) conducting an ultrasonic wave washing of said polished surface employing a washing liquid; and (ii) conducting a physical washing of said polished surface after the ultrasonic wave washing.

12. (Amended) A fabrication method of a semiconductor device according to claim 11, wherein said polishing step is conducted employing chemical mechanical polishing.

13. (Unamended From Previous Version) A fabrication method of a semiconductor device according to claim 11, wherein said ultrasonic wave washing is carried out at a frequency band of not less than 800 kHz.

14. (Unamended From Previous Version) A fabrication method of a semiconductor device according to claim 13, wherein said frequency band is a range of 1 MHz to 3 MHz.

15. (Unamended From Previous Version) A fabrication method of a semiconductor device according to claim 11, wherein said ultrasonic wave washing is carried out while said washing liquid is discharged from a nozzle.

16. (Unamended From Previous Version) A fabrication method of a semiconductor device according to claim 11, wherein said ultrasonic washing is carried out while the substrate with said polished surface thereon is rotated at 1000-2500 rpm.

17. (Unamended From Previous Version) A fabrication method of a semiconductor device according to claim 11, wherein said physical washing is conducted by brush scrubbing or high-pressure jet washing.

18. (Unamended From Previous Version) A fabrication method of a semiconductor device according to claim 11, wherein said physical washing is carried out using a sponge.

19. (Unamended From Previous Version) A fabrication method of a semiconductor device according to claim 18, wherein said sponge comprises polyvinyl alcohol.

20. (Unamended From Previous Version) A fabrication method of a semiconductor device according to claim 11, wherein ultrasonic washing is repeated after said physical washing.

21 to 24. Cancelled.

25. (Amended) A fabrication method according to claim 11, wherein said metal film is Al, Cu, Au, Cr, Mo, Pt, Ti or an alloy thereof.

26. (Unamended From Previous Version) A fabrication method according to claim 25, wherein said alloy is AlSi, AlCu or AlSiCu.

27. (Amended) A fabrication method according to claim 11, including forming a barrier metal prior to forming the metal film.

28 to 29. Cancelled.

30. (Unamended From Previous Version) A fabrication method according to claim 11, wherein said polishing step is performed by a polishing with a slurry containing an abrasive.

31. (Unamended From Previous Version) A fabrication method according to claim 11, wherein said washing liquid is pure water.

32. (Unamended From Previous Version) A fabrication method according to claim 11, wherein the ultrasonic wave washing is conducted to reduce an amount of abrasive particles adhered to the polished surface and, thereafter, the amount of abrasive particles is further reduced by the physical washing.

33 to 44. Cancelled.

45. (New) A process for producing a semiconductor device comprising:

a first step of forming a first insulating film on a substrate, said substrate having a semiconductor region;

a second step of forming a second insulating film on the substrate, said second insulating film being of a different material than the first insulating film and serving as a polishing stopper;

a third step of forming by an etching process an opening in the second insulating film, wherein a part of the second insulating film remains within said opening;

a fourth step of forming a metal film on the second insulating film and the opening, wherein the metal film has a polishing rate greater than that of the second insulating film; and

a fifth step of polishing the metal film to expose a surface of the second insulating film etched in the third step and to form a flat plane comprising the exposed surface of the second insulating film and a polished surface of the metal film.

46. (New) The process according to Claim 45, further comprising a step of forming a third insulating film serving as an etching stopper on the first insulating film after the second step and before the third step.

47. (New) The process according to Claim 45, further comprising a step of causing the first insulating film used in the first step to serve as a gate insulating film, forming a transistor by the gate insulating film and the semiconductor region, connecting the metal film having the polished surface in the fifth step to a drain region of the formed transistor, and forming an active matrix device causing the metal film to serve as a reflection electrode.

48. (New) The process according to any of Claims 45 to 47, wherein the metal film is made of aluminum and the second insulating film is made of silicon oxide.

49. (New) The process according to Claim 46, wherein the metal film is made of aluminum and the second insulating film is made of silicon oxide and the third insulating film is made of silicon nitride.

50. (New) The process according to any of Claims 45 to 47, wherein the step of polishing comprises a step using CMP.

51. (New) The process according to any of Claims 45 to 47, wherein the semiconductor region comprises polysilicon.

52. (New) The process according to any of Claims 45 to 47, wherein the part of the second insulating film remaining in said opening has a columnar shape.

53. (New) The process according to Claim 45, wherein the etching process used in the third step is a dry etching process.

54. (New) The process according to Claim 45, wherein the etching process used in the third step is a wet etching process.